REMARKS

Claims 1-7 and 9-20 are pending in the present application.

Claim Rejections-35 U.S.C. 103

Claims 11-14 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Arase reference (Japanese Patent Publication No. 4-69939) in view of the Schuele et al. reference (U.S. Patent No. 5,717,250). This rejection is respectfully traversed for the following reasons.

The semiconductor device of claim 11 includes in combination a silicon substrate; an impurity region; a first insulating film; a polysilicon plug "of a second conductivity type formed in the first opening in contact with the impurity region and on an upper surface of the first insulating film"; a second insulating film "formed on an upper surface of the polysilicon plug and on the upper surface of the first insulating film, the second insulating film having a second opening over the polysilicon plug"; and a conductive wiring layer "formed in the second opening in contact with the polysilicon plug and on an upper surface of the second insulating film". Applicant respectfully submits that the semiconductor device of claim 11 would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

The Examiner has relied upon the Arase reference as in the previous Office Action dated December 1, 2005. The Examiner has acknowledged that the Arase reference fails to disclose first and second insulating layers and their required

relationships with the silicon plug, as would be necessary to meet the features of claim 11.

In an effort to overcome the acknowledged deficiencies of the Arase reference, the Examiner has alleged that Schuele et al. "disclose a sputter and CVD deposited titanium nitride barrier layer between a platinum layer and a polysilicon plug where in Fig. 6, insulating layer 63 formed on an upper surface of the polysilicon plugs both labeled as 16". The Examiner has alleged that it would have been obvious "to include the required first and second insulating films with their required relationship to polysilicon plug in Arase as taught by Schuele et al. in order to have a semiconductor device with better insulation characteristics".

As noted above, the Examiner has acknowledged that the Arase reference has failed to disclose first and second insulating layers and their required relationship with a polysilicon plug. The Examiner has consequently made specific reference to "insulating layer 63" in Fig. 6 of the Schuele et al. reference. The Examiner has however failed to specify on the record how the structure in Fig. 6 of the Schuele et al. reference has been interpreted to include both first and second insulating films as featured in claim 11. As noted, the Examiner has made reference to only a single layer in the Schuele et al. reference. This rejection is thus incomplete and unclear fro at least these reasons.

Applicant presumes that the Examiner has interpreted BPSG dielectric layer 14 and capacitor dielectric 63 in Fig. 6 of the Schuele et al. reference respectively as the first and second insulating films of claim 11. The following comments are offered in

view of this understanding.

Applicant respectfully submits that BPSG dielectric layer 14 and capacitor dielectric 63 in Fig. 6 of the Schuele et al. reference cannot be respectively interpreted as the first and second insulating films of claim 11. Particularly, the polysilicon plug of claim 11 is featured as "on an upper surface of the first insulating film". However, as shown in Fig. 6 of the Schuele et al. reference, polysilicon plug 16 is formed recessed in an opening in BPSG dielectric layer 14, and clearly is not formed on an upper surface of BPSG dielectric layer 14, as would be necessary to meet the features of claim 11. BPSG dielectric layer 14 of the Schuele et al. reference therefore cannot be interpreted as the first insulating film of claim 11. The Schuele et al. reference thus fails to meet the features of claim 11, and consequently fails to overcome the acknowledged deficiencies of the primarily relied upon Arase reference. Applicant therefore respectfully submits that the semiconductor device of claim 11 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 11-14 is improper for at least these reasons.

With further regard to this rejection, the second insulating film of claim 11 is featured as "having a second opening over the polysilicon plug". Since capacitor dielectric 63 is shown in Fig. 6 of the Schuele et al. reference as formed over the entire upper surface of the structure, capacitor dielectric 63 clearly fails to include an opening over polysilicon plug 16, as would be necessary to meet the further features of claim 11. Capacitor dielectric 63 of the Schuele et al. reference therefore cannot be

interpreted as the second insulating film of claim 11. The Schuele et al. reference thus fails to meet the features of claim 11, and consequently fails to overcome the acknowledged deficiencies of the primarily relied upon Arase reference. Applicant therefore respectfully submits that the semiconductor device of claim 11 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection of claims 11-14 is improper for at least these additional reasons.

With further regard to this rejection, the conductive wiring layer of claim 11 is featured as "formed in the second opening in contact with the polysilicon plug and on an upper surface of the second insulating film". Assuming for the sake of argument that titanium silicide 61, titanium carbonitride 41, titanium nitride layer 42 and platinum lower capacitor electrode 62 could broadly be collectively interpreted as a conductive wiring layer, these layers taken singularly or together are not shown in Fig. 6 of the Schuele et al. reference as formed on an upper surface of capacitor dielectric 63, as would be necessary to meet the features of claim 11. That is, since platinum lower capacitor electrode 62 is not formed on capacitor dielectric 63, platinum lower capacitor electrode 62 and capacitor dielectric 63 cannot be respectively interpreted as the conductive wiring layer and the second insulating film of claim 11. The Schuele et al. reference as apparently relied upon therefore does not overcome the deficiencies of the primarily relied upon Arase reference. Applicant therefore respectfully submits that the semiconductor device of claim 11 would not have been obvious in view of the prior art

as relied upon by the Examiner taken singularly or together, and that this rejection of claims 11-14 is improper for at least these additional reasons.

Finally, the Examiner has apparently asserted that the use of first and second insulating layers as allegedly taught by the Schuele et al. reference would provide in the Arase reference a semiconductor device "with better insulation characteristics". However, it is not clear how such a teaching could be drawn from the Schuele et al. reference, because the Examiner has referred to a capacitor dielectric 63 only in the Schuele et al. reference. Moreover, it is not clear how or why one of ordinary skill would be motivated to use a capacitor dielectric (which necessarily would be implemented between a pair of capacitor electrodes) to enable "better insulation characteristics" of a polysilicon plug. Applicant respectfully submits that the Examiner has failed to establish the necessary motivation to modify the primarily relied upon Arase reference in view of the Schuele et al. reference, and that this rejection is improper for at least these further reasons.

Allowable Subject Matter

Applicant respectfully notes the Examiner's acknowledgment that claims 1-7, 9, 10 and 16-20 are allowed. However, since claim 16 is dependent upon claim 11 (which currently stands rejected), the Examiner is respectfully requested to confirm the status of claim 16.

Applicant also respectfully notes the Examiner's acknowledgement that claim 15

has been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. However, since claim 11 should be considered allowable for at least the reasons as set forth above, Applicant respectfully submits that amendment of claim 15 to be in independent form is unnecessary.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

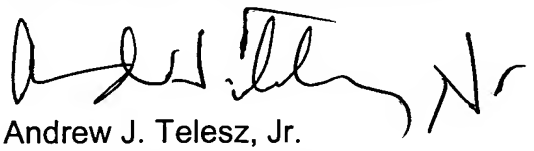
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicant hereby petitions for an extension of one (1) month to September 22, 2006, for the period in which to file a response to the outstanding Office Action. The required fee of $120.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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